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(54) Method and apparatus for reducing power supply current surges in a charge pump using a delayed clock line

(57) The present invention is a charge pump circuit to reduce and distribute power supply current surges. The charge pump circuit includes a first clock line to provide a first clock thereon, a plurality of delay circuits connected in series, each delay circuit generating a delayed and inverted clock from its input clock on a respective output clock line, and a plurality of charge pump stages

connected in series each to store charge thereon. The first clock line is coupled to the first charge pump stage and the plurality of output clock lines are coupled to a respective plurality of remaining charge pump stages. The operation of each charge pump stage is staggered to reduce and distribute the power supply current surges.

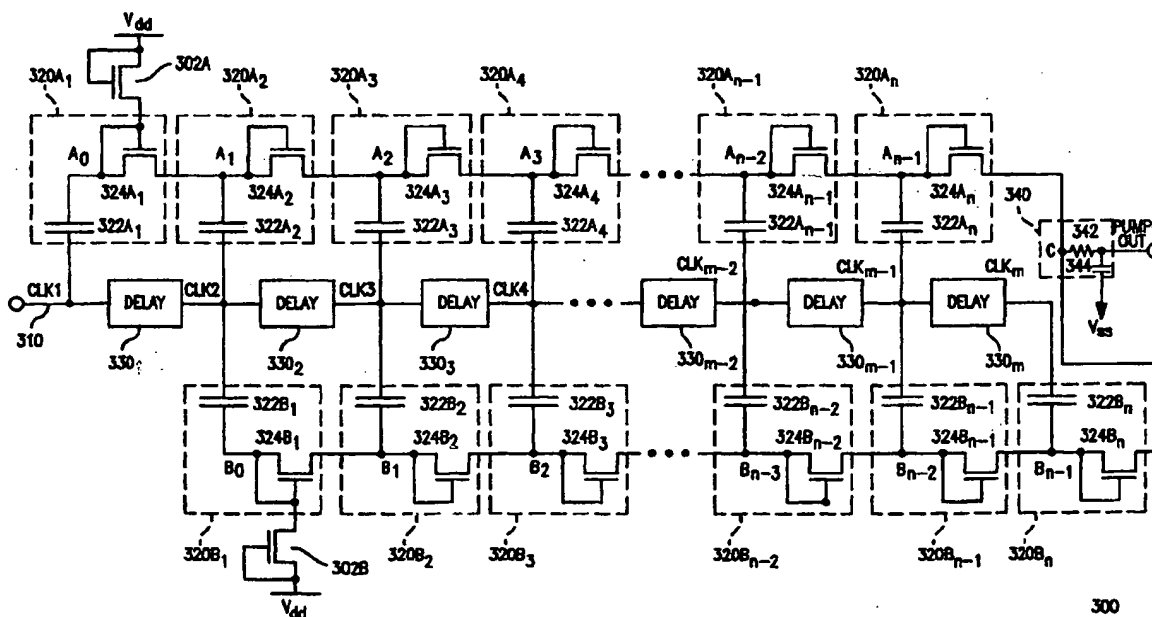


FIG. 3A

300

## Description

### 1. Field of the Invention

[0001] The present invention relates to charge pumps, and methods and apparatus for reducing power supply current surges in a charge Pump.

### 2. Description of Related Art

[0002] Patent number 5,629,890 to Engh relates to an integrated circuit system for analog signal storage which incorporates a read-while-write programming method. In the read-while-write programming method of the '890 patent, a high voltage ramp is applied to a memory cell to program the memory cell to a target voltage. Figure 1 illustrates the charge pump circuit 100 that provides the high output voltage during writing/programming of a memory cell. As shown in Figure 1, the charge pump circuit 100 includes two charge pump lines, each charge pump line having a plurality of charge pump stages 110A<sub>1</sub>-110A<sub>n</sub> and 110B<sub>1</sub>-110B<sub>n</sub>, respectively. Each of the charge pump stages 110A<sub>1</sub>-110A<sub>n</sub> and 110B<sub>1</sub>-110B<sub>n</sub> includes a respective capacitor CA<sub>1</sub>-CA<sub>n</sub> and CB<sub>1</sub>-CB<sub>n</sub>, and a respective N-channel device MA<sub>1</sub>-MA<sub>n</sub> and MB<sub>1</sub>-MB<sub>n</sub>, each connected as a diode. A plurality of clock sources CLK1, CLK1B, CLK2, and CLK2B are provided, with alternate stages of each charge pump being connected to a common clock signal.

[0003] Figure 2A illustrates a timing diagram of the prior art charge pump clock signals. As can be seen from the Figure, clock signals CLK1 and CLK1B, as well as clock signals CLK2 and CLK2B, are non-overlapping. Thus, clock signals CLK1 and CLK1B are never both high at the same time, and clock signals CLK2 and CLK2B are never both high at the same time. The operation of the circuit of Figure 1 may be described as follows. (In this description, it will be assumed that the diode voltage drop of all of the diode-connected transistors in Figure 1 is equal to  $V_d$  and that the clock signals swing between zero or ground and  $V_{dd}$ .) When clock signal CLK1 is low, capacitor CA1 will charge to a voltage  $V_{dd}-V_d$ , where  $V_d$  is the diode voltage drop of diode-connected transistor MA<sub>0</sub>. When clock signal CLK1 goes high, the voltage at node A<sub>0</sub> will rise toward  $2V_{dd}-V_d$ . If the voltage at node A<sub>1</sub> is presently less than  $2V_{dd}-2V_d$  (clock signal CLK1B being low), diode-connected transistor MA<sub>1</sub> will become forward biased, dumping some of the charge from capacitor CA<sub>1</sub> to capacitor CA<sub>2</sub>.

[0004] On the other hand, if the voltage at node A<sub>1</sub> is just equal to  $2V_{dd}-2V_d$ , diode-connected transistor MA<sub>2</sub> will be just on the threshold of conducting, though no substantial charge will be transferred from capacitor CA<sub>1</sub> to capacitor CA<sub>2</sub>. When the clock signal CLK1 goes low again, diode-connected transistor MA<sub>1</sub> will be reverse biased. When clock signal CLK1B goes high, the voltage on node A<sub>1</sub> will increase from  $2V_{dd}-2V_d$  toward  $3V_{dd}-2V_d$ . If at this time the voltage on node A<sub>2</sub> is less

than  $3V_{dd}-3V_d$ , part of the charge from capacitor CA<sub>2</sub> will be dumped into capacitor CA<sub>3</sub>. If, on the other hand, the voltage on node A<sub>2</sub> is just equal to  $3V_{dd}-3V_d$ , diode-connected transistor MA<sub>2</sub> will be just on the threshold of conducting, though again no substantial charge will be transferred from capacitor CA<sub>2</sub> to capacitor CA<sub>3</sub>. Thus, carrying out this analysis to the limit, it may be seen that for n charge pump stages, the charge pump voltage limit for an unloaded (open circuit) charge pump output will be equal to  $N(V_{dd}-V_d)$ .

[0005] For any real load on the charge pump, output capacitor CA<sub>n</sub> and CB<sub>n</sub> will discharge somewhat between pumping cycles to provide the output current into the load, in which case each stage of the two charge pump lines will pump charge toward the output at a rate dependent upon the charge pump output current. Accordingly, the charge pump circuit will appear as a voltage source with a source impedance inversely proportional to the size of the capacitors times the frequency of the clock signals.

[0006] In the read-while-write programming method, a read operation is simultaneously performed while the memory cell is being programmed to determine when to terminate the application of the high voltage (i.e., when the target voltage is reached). Since the reading occurs during the writing operation, the charge pump circuit 100 of Figure 1 is active when the voltage stored on the cell is being read back. Depending on the number of charge pump stages, the loading on each of the clock drivers of the prior art is relatively large, being proportional to  $(n^2C)/2$ , where n is the number of charge pump stages and C is the value of each capacitor. Driving a large load requires a large clock driver, which in turn increases the demand on the power supply. Large demands on the power supply cause current surges which cause undesirable disturbances in the system. Figure 2B schematically illustrates the current surges on the power supply with reference to clocks CLK1, CLK1B, CLK2, and CLK2B.

[0007] The large current surges can result in inaccurate reading of the memory cell in the read-while-write programming method. As a result, the memory cell may be underprogrammed or overprogrammed. Also with the prior art charge pump, additional circuitry is needed to ensure that clocks CLK1 and CLK1B are non-overlapping and clocks CLK2 and CLK2B are non-overlapping. Further, as the demand continues for smaller die sizes, new design techniques and system implementations are needed to reduce the die area for any intended function.

[0008] Accordingly, there is a need in the art for an apparatus and method of providing a high voltage charge pump that outputs a high voltage while reducing instantaneous power supply current surges and reducing the overall size of the circuit.

## SUMMARY OF THE INVENTION

**[0009]** The present invention is a charge pump circuit to reduce and distribute power supply current surges. The charge pump circuit includes a first clock line to provide a first clock thereon, a plurality of delay circuits connected in series, each delay circuit generating a delayed and inverted clock from its input clock on a respective output clock line, and a plurality of charge pump stages connected in series each to store charge thereon. The first clock line is coupled to the first charge pump stage and the plurality of output clock lines are coupled to a respective plurality of remaining charge pump stages. The operation of each charge pump stage is staggered to reduce and distribute the power supply current surges.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0010]** The features and advantages of the present invention will become apparent from the following detailed description of the present invention in which

Figure 1 illustrates a prior art charge pump circuit.

Figure 2A illustrates a timing diagram of the prior art charge pump clock sources

Figure 2B illustrates the power supply current surges of the prior art charge pump circuit

Figure 3A illustrates one embodiment of the charge pump circuit of the present invention

Figures 3B illustrates a timing diagram for the clock signals used in the preferred embodiment charge pump circuit of the present invention

Figure 3C illustrates individual driver current surges on the power supply of the charge pump circuit of the present invention.

Figure 3D illustrates combined driver current surges on the power supply of the charge pump circuit of the present invention.

Figures 4 illustrates one embodiment of the delay circuit used in the preferred embodiment of the present invention.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

**[0011]** First referring to Figure 3A, the preferred embodiment of the charge pump circuit 300 of the present invention may be seen. The charge pump circuit 300 includes a clock signal line 310 that provides a clock signal CLK1, first and second charge pumps or charge pump

lines, each comprising a series of charge pump stages 320A<sub>1</sub>-320A<sub>n</sub> and 320B<sub>1</sub>-320B<sub>n</sub>, respectively, a plurality of identical inverting delay clock circuits 330<sub>1</sub>-330<sub>m</sub>, and a low pass filter circuit 340 to provide a filtered output, PUMPOUT, of the charge pump circuit. Each stage of the first charge pump lines 320A<sub>1</sub>-320A<sub>n</sub> includes one capacitor 322A<sub>1</sub>-322A<sub>n</sub> and one N-channel device 324A<sub>1</sub>-324A<sub>n</sub>, each of which is diode-connected. Similarly, each stage of the second charge pump lines 320B<sub>1</sub>-320B<sub>n</sub> includes one capacitor 322B<sub>1</sub>-322B<sub>n</sub> and one N-channel device 324B<sub>1</sub>-324B<sub>n</sub>, each of which is also diode-connected.

**[0012]** As may be seen in Figure 3A, charge pump stage 320A<sub>1</sub> is driven by the clock signal CLK1. Charge pump stages 320A<sub>2</sub> and 320B<sub>2</sub> are driven by clock signal CLK2, delayed and inverted by delay 330<sub>1</sub> with respect to clock signal CLK1. Each stage of the series of stages in the upper charge pump line is similarly driven as successively delayed and inverted clock signals, as is illustrated in Figure 3B. The lower series of charge pump stages shown in Figure 3A are also driven by clock signals each delayed and inverted with respect to the clock signal driving the prior stage of the charge pump line. The first stage 320B<sub>1</sub> of the lower charge pump line, however, is driven not by the clock signal CLK1 but rather by the delayed and inverted clock signal CLK2, so that whatever happens in the upper charge pump line will similarly happen in the lower charge pump line, though time delayed with respect thereto.

**[0013]** In operation under a normal load, first assume the clock signal CLK1 is low, as shown in Figure 3B. Capacitor 322A<sub>1</sub> will charge through diode-connected transistor 302A to the voltage  $V_{dd}-V_d$ . Then when the clock signal CLK1 goes high, node A<sub>0</sub> will be encouraged toward the voltage  $2V_{dd}-V_d$ . As may be seen from Figure 3B, at this time the delayed and inverted clock signal CLK2 will still be high. Unless the voltage of node A<sub>1</sub> at this time is less than  $2V_{dd}-2V_d$ , diode-connected transistor 324A<sub>1</sub> will not be forward biased and no charge will be transferred from capacitor 322A<sub>1</sub> to capacitor 322A<sub>2</sub>. However, when the delayed and inverted clock signal CLK2 then goes low, diode-connected transistor 324A<sub>1</sub> will become forward biased and part of the charge on capacitor 322A<sub>1</sub> will be transferred to capacitor 322A<sub>2</sub>, raising the voltage of node A<sub>1</sub>.

**[0014]** Similarly, when the delayed and inverted clock signal CLK2 goes high again, the voltage at node A<sub>1</sub> will be encouraged further upward by an increment  $V_{dd}$ . At this time, the further delayed and inverted clock signal CLK3 will still be high, and again unless the voltage at node A<sub>2</sub> is now less than the then existing voltage at node A<sub>1</sub> by at least  $V_{dd}$ , no part of the charge will be transferred from capacitor 322A<sub>2</sub> to capacitor 322A<sub>3</sub>. However, when the further delayed and inverted clock signal CLK3 goes low, diode-connected transistor 324A<sub>2</sub> will become forward biased and part of the charge from capacitor 322A<sub>2</sub> will be transferred to capacitor 322A<sub>3</sub>, raising the voltage of node A<sub>3</sub>.

[0015] Since in the steady state the average voltage at each of the nodes  $A_0$  through  $A_{n-1}$  doesn't change, it is apparent that the charge transferred from capacitor 322A<sub>1</sub> to capacitor 322A<sub>2</sub> on a charge pumping cycle of stage 320A<sub>1</sub> will be equal to the charge transferred from capacitor 322A<sub>2</sub> to capacitor 322A<sub>3</sub> on a charge pumping cycle of stage 320A<sub>2</sub>, etc. However, these charge pumping cycles for each stage of the n stages of the upper charge pump line of Figure 3A are delayed, one to another, or staggered, so that the current spike loads on the power supply for generating the clock signals are similarly staggered (see Figures 3C and 3D). In particular, in the prior art, given the two interleaved charge pump lines, each having n stages, each clock signal would drive n capacitors at a time. In comparison, only two capacitors are driven at a time in the circuit of Figure 3A, the driving of all 2n capacitors being spread out over n time increments, wherein each time increment equals the delay of one of the delay circuits 330. Consequently, while the circuit of Figure 3A might, for instance, operate at the same clock frequency (preferably higher) as that of the prior art, the instantaneous loading on the power supply is greatly reduced and the frequency of the power supply current ripple is substantially increased, making the filtering of the ripple easier and more effective.

[0016] Referring again to Figure 3A, it may be seen that when the clock signal CLK1 goes low, whatever charge had been transferred to capacitor 322A<sub>2</sub> from capacitor 322A<sub>1</sub>, now lowering the voltage of capacitor 322A<sub>1</sub> to below  $V_{dd} - V_d$ , will be replenished from the power supply through diode-connected transistor 302A. Accordingly, while the pumping action resulting from any clock signal going high puts a load on the power supply to drive that clock signal, the replenishment of the charge on capacitor 322A<sub>1</sub> will also put some load on the power supply when the clock signal CLK1 goes low. While the first stage 322B<sub>1</sub> of the lower charge pump line could have been driven by the signal CLK1, the staggering and inverting of the drive of this stage also avoids the simultaneous replenishment of the charge of capacitors 322A<sub>1</sub> and 322B<sub>1</sub> in preparation for the next charge pumping operation. This, too, reduces the magnitude of the current spikes on the power supply. The inverting of the charge pump line starting signals also interleaves the output of the charge pump lines, reducing the output ripple voltage and increasing its frequency for easier filtering.

[0017] Figure 4 illustrates one embodiment of the delay circuit 400 of the present invention. Referring to Figure 4, the delay circuit 400 includes P-channel MOS devices 404, 408, 410 and 416 and N-channel MOS devices 406, 412, 414 and 418. The delay circuit 400 receives an input clock signal CLKIN on an input signal line 402, delays the input clock signal CLKIN by a predetermined amount of time, and provides an inverted output clock signal CLKOUT on an output signal line 420. More specifically, when the input clock signal CLKIN goes low, N-channel device 406 turns off and P-

channel device 404 turns on, causing node A to be pulled high to  $V_{dd}$ . With node A at  $V_{dd}$ , P-channel devices 408 and 410 turn off and N-channel devices 412 and 414 turn on. With N-channel device 412 turned on, node B is pulled down to  $V_{ss}$  and causes N-channel device 418 to turn off. With N-channel device 414 turned on, node C is also pulled down to the voltage at node B which is  $V_{ss}$ . This causes P-channel device 416 to turn on. As such, the output clock signal CLKOUT is pulled high to  $V_{dd}$ . N-channel device 414 assures that transistor 418 turns off before transistor 416 turns on, preventing both transistors from being on momentarily during the switching.

[0018] Conversely, if the input clock signal CLKIN goes high, P-channel device 404 turns off and N-channel device 406 turns on, causing node A to be pulled low to  $V_{ss}$ . With node A at 0 volts (or close to 0 volts), N-channel devices 412 and 414 are turned off and P-channel devices 408 and 410 are turned on. With both P-channel devices 408 and 410 on, node B is first pulled high to  $V_{dd}$ , thus causing P-channel device 416 to turn off. Thereafter, node B is pulled high to  $V_{dd}$ , thereby causing N-channel device 418 to turn on. With N-channel device 418 turned on, the output clock signal CLKOUT is pulled low to  $V_{ss}$ . Now, P-channel device 410 assures that transistor 416 turns off before transistor 418 turns on, again preventing both transistors from being on momentarily during the switching. Thus, the delay circuit 400 inverts and delays an input clock signal as stated.

[0019] In the preferred embodiment, the delay circuits 330<sub>1</sub>-330<sub>M</sub> are analog delay and inverting circuits, specifically successive inverter type circuits which merely impose a delay based upon the response time of the circuit. In other embodiments, however, the clock signal CLK1 might be digitally generated, such as by way of example, dividing down a frequency n times the clock frequency CLK1, with each count of the higher frequency initiating the next successive delayed and inverted clock cycle. In this way, the M delayed and inverted clock signals may be equally staggered throughout the cycle time of one clock cycle CLK1 to maximize the smoothing effect of the present invention. Further, in such an embodiment, the charge pump stage 320B<sub>1</sub> might be driven from the delayed clock signal CLK<sub>M2</sub>, with each subsequent stage being driven by the next subsequent delayed and inverted clock signal, using wrap-around to provide the full series of M delayed and inverted clock cycles. Such an embodiment would both equally stagger the replenishment of the charge on capacitors 322A<sub>1</sub> and 322B<sub>1</sub> and equally stagger the pumping of the two charge pump lines to the output filter and load. However, the reduction in the power supply current spikes beyond that of the prior embodiment disclosed would not be substantial.

[0020] As pointed out previously, each clock signal generated by a delay circuit is inverted and delayed with respect to the input to the delay circuit. (Preferably, the

total delay imposed by the combination of all delay circuits is at least one-half the period of clock signal CLK1 for best performance.) As a result, not only are the current supply surges distributed over time, but the load on each clock driver (i.e., delay circuit) is small, so that the clock drivers may be small. Also, any switching current required by the delay circuits are spread out over time. Thus, the amplitude of the power supply current surges is small, and at a higher frequency, as shown in Figures 3C and 3D. This is to be distinguished from the prior art where large, lower frequency power supply current surges occur when the clock drivers are switching, and of course, the prior art clock drivers had to be large to drive the larger capacitive loads.

[0021] As a result of the foregoing, the present invention provides a quieter system over the prior art, and alleviates the problem with the prior art of underprogramming or overprogramming a memory cell during the read-while-write programming method. In addition, the prior art charge pump circuit requires circuitry for ensuring that clocks CLK1 and CLK1B are non-overlapping as well as CLK2 and CLK2B, as opposed to the present invention where no such circuit is needed.

[0022] To further reduce the area of the charge pump circuit 300 of Figure 3A, the capacitors are made smaller and the clock frequency is increased, as the capacitance value of each capacitor is inversely proportional to the clock frequency for the same pumping capacity. This in turn requires still smaller delay clock drivers to drive the smaller capacitors. Increasing the clock frequency and decreasing the capacitor size increases the frequency of the output voltage ripple and decreases the amplitude of the output ripple, making the filtering of the charge pump output by resistor 342 and capacitor 344 easier and more effective.

[0023] With the present invention, the current surges on the power supply are reduced and distributed due to smaller clock drivers and smaller loads. Moreover, through the use of increased clock frequency and smaller capacitors, the overall size of the circuit is further reduced. This also reduces the output ripple, and provides for a quieter system and enhanced system performance.

[0024] While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and arrangements shown and described, since various other modifications may readily occur to those ordinarily skilled in the art.

#### Claim

1. A charge pump circuit to reduce power supply current surges, comprising:

a first clock line to have a first clock signal thereon;  
 a first charge pump circuit to store a first charge thereon and coupled to said first clock source to output a first voltage in response to said first clock signal;  
 a first delay circuit coupled to said first clock line to delay and generate a second clock signal on a second clock line;  
 a second charge pump circuit to store a second charge thereon and coupled to said first charge pump circuit and said first delay circuit, said second charge pump circuit to generate a second voltage in response to said second clock signal,  
 wherein the operation of the second charge pump stage is staggered with respect to the operation of the first charge pump stage to reduce and distribute power supply current surges.

2. The charge pump circuit of claim 1 wherein when said first clock signal is active and said second clock signal is inactive, a first portion of the first charge on said first charge pump circuit is transferred to said second charge pump circuit.

3. The charge pump circuit of claim 1 further comprising:

a second delay circuit coupled to said first delay circuit to delay and generate a third clock signal on a third clock signal line; and  
 a third charge pump circuit coupled to said second charge pump circuit and said second delay circuit, said third charge pump circuit to output a third voltage in response to said third clock signal,  
 wherein when said second clock signal is active and said third clock signal is inactive, a second portion of the second charge is transferred to said third charge pump circuit.

4. The charge pump circuit of claim 1 wherein each of said first and second charge pump circuits includes:

a capacitor coupled to one of said first or second clock lines; and  
 a N-channel device configured as a diode having an input and an output, said input of said N-channel device being coupled to said capacitor, said output of said N-channel device being coupled to said second charge pump circuit or an output terminal.

5. The charge pump circuit of claim 2 wherein said second clock signal is inverted and delayed by a predetermined amount of time from said first clock signal.

6. A charge pump circuit to reduce and distribute power supply current surges, comprising:

a first clock line to provide a first clock thereon;  
a plurality of delay circuits connected in series,  
each delay circuit generating a delayed and inverted clock from its input clock on a respective output clock line; and

a plurality of charge pump stages connected in series each to store charge thereon, the first clock line being coupled to the first charge pump stage and the plurality of output clock lines being coupled to a respective plurality of remaining charge pump stages,

wherein the operation of each charge pump stage is staggered to reduce and distribute the power supply current surges

7. The charge pump circuit of claim 6 wherein charge is transferred from one charge pump stage to a next charge pump stage when a clock of the one charge pump stage is active and the clock of the next charge pump stage is inactive

8. The charge pump circuit of claim 6 wherein each charge pump stage comprises

a capacitor coupled to a clock or a first clock line; and

a N-channel device configured as a diode having an input and an output, said input of said N-channel device being coupled to said capacitor, said output of said N-channel device being coupled to a next charge pump stage.

9. A method of reducing and distributing power supply current surges in a charge pump circuit having a first clock, a plurality of delay circuits, a plurality of charge pump stages, and an output terminal coupled to a last charge pump stage, comprising the steps of:

(a) providing the first clock to the first charge pump stage and the first delay circuit;

(b) the plurality of delay circuits generating a plurality of clocks, each of which is delayed and inverted with respect to its input clock;

(c) providing the plurality of clocks to a respective plurality of remaining charge pump stages; and

(d) transferring charge from one charge pump stage to a next charge pump stage when the clock for the one charge pump stage is active and the clock for the next charge pump stage is inactive,

wherein the operation of each charge pump stage is staggered with respect to the previous

charge pump stage to reduce and distribute the power supply current surges.

10. The method of claim 9, wherein each charge pump stage comprises:

a capacitor coupled to a clock or a first clock; and

a N-channel device configured as a diode having an input and an output, said input of said N-channel device being coupled to said capacitor, said output of said N-channel device being coupled to a next charge pump stage.

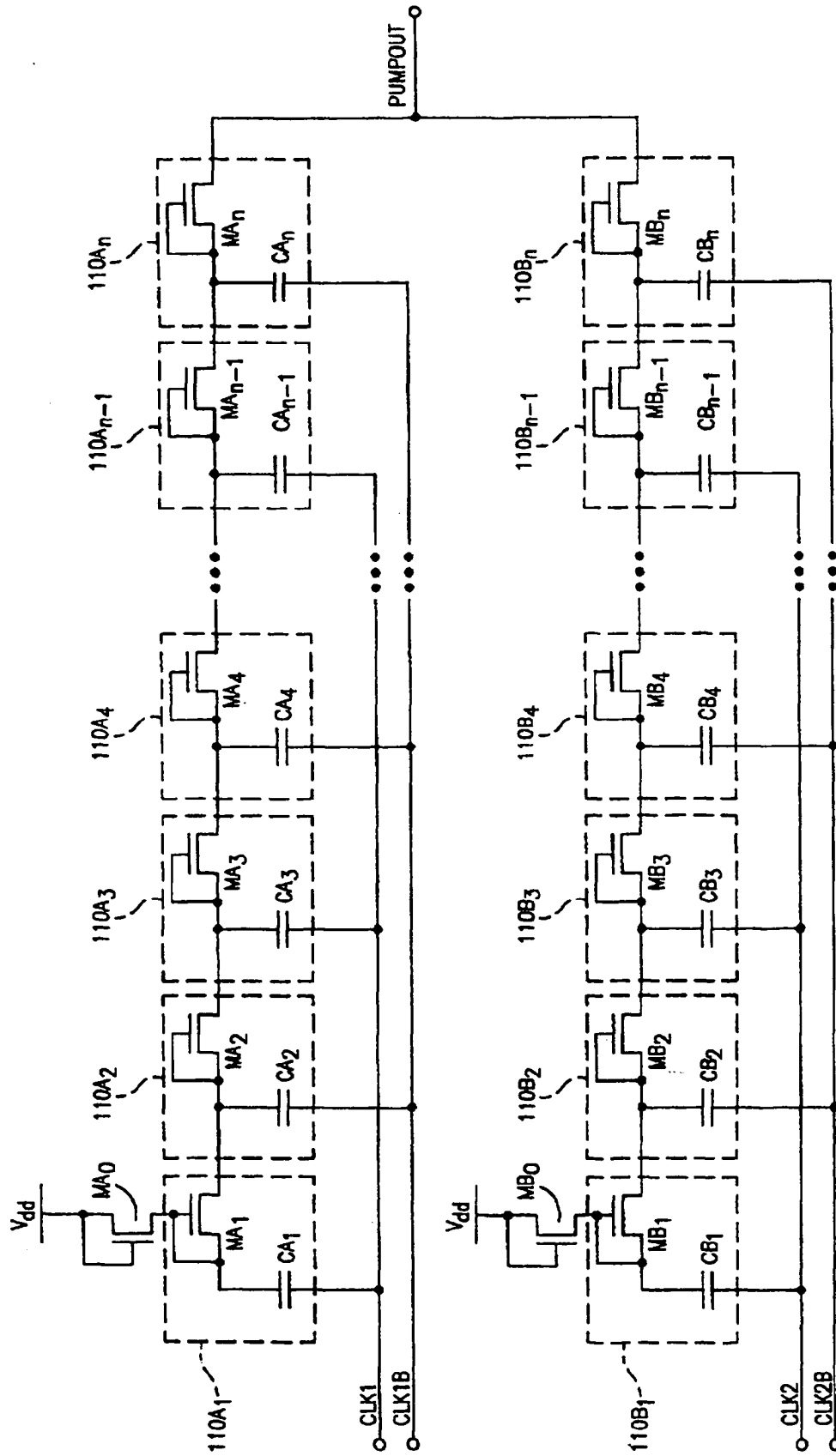
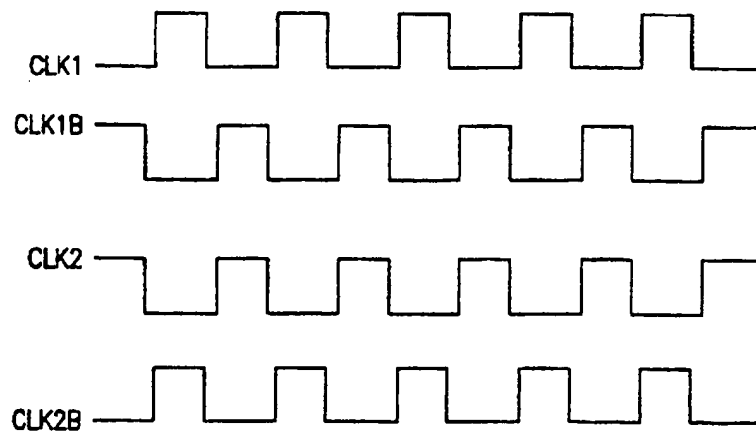
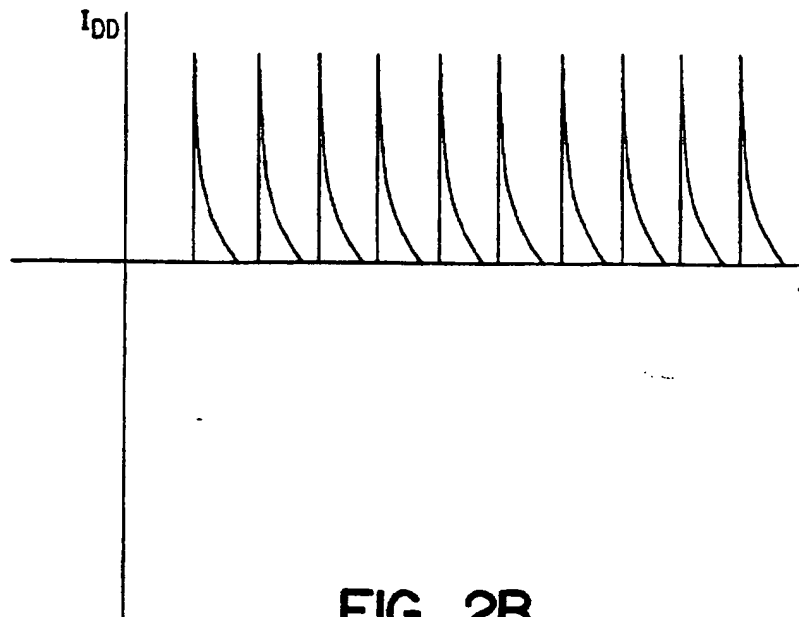


FIG. 1  
PRIOR ART



**FIG. 2A**  
PRIOR ART



**FIG. 2B**  
PRIOR ART

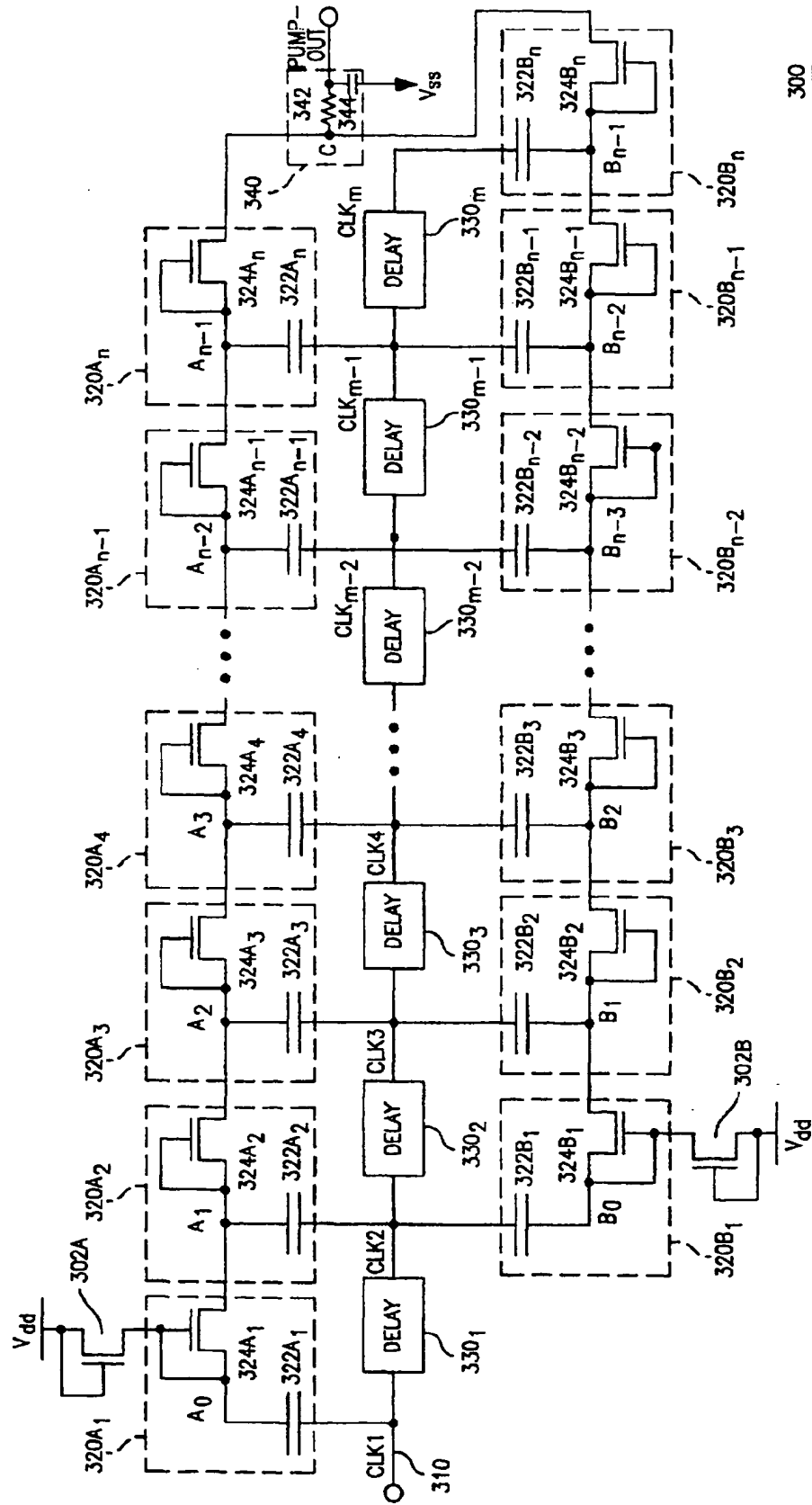


FIG. 3A

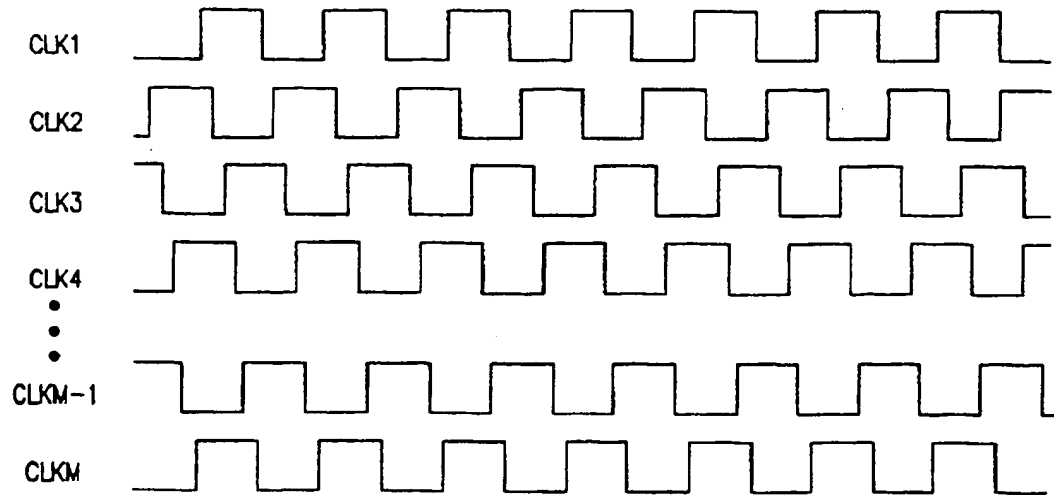


FIG. 3B

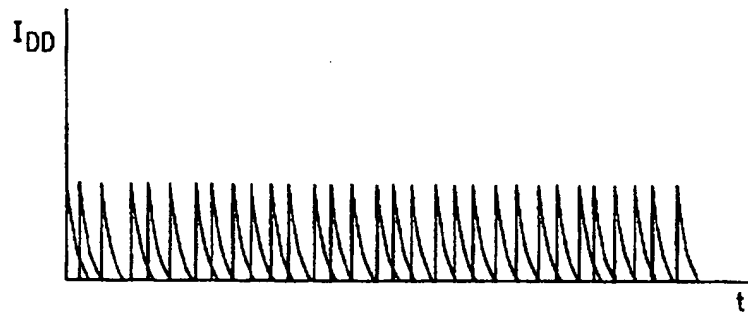


FIG. 3C

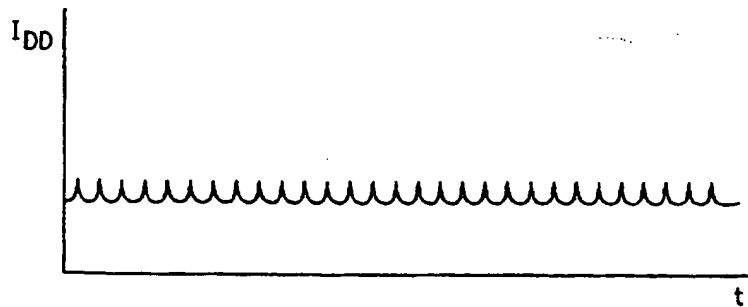


FIG. 3D

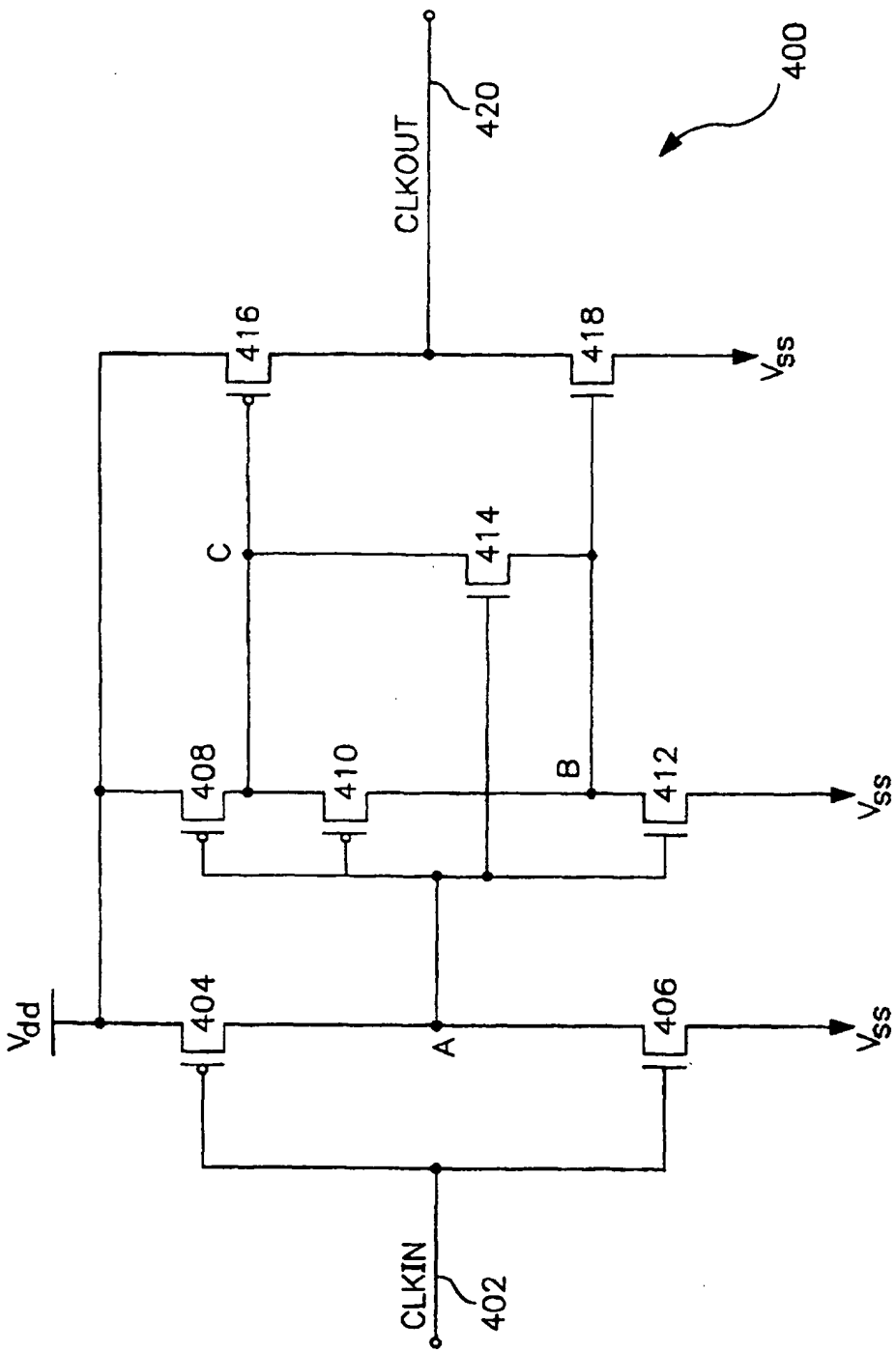
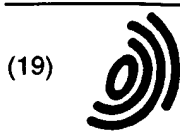


FIG. 4



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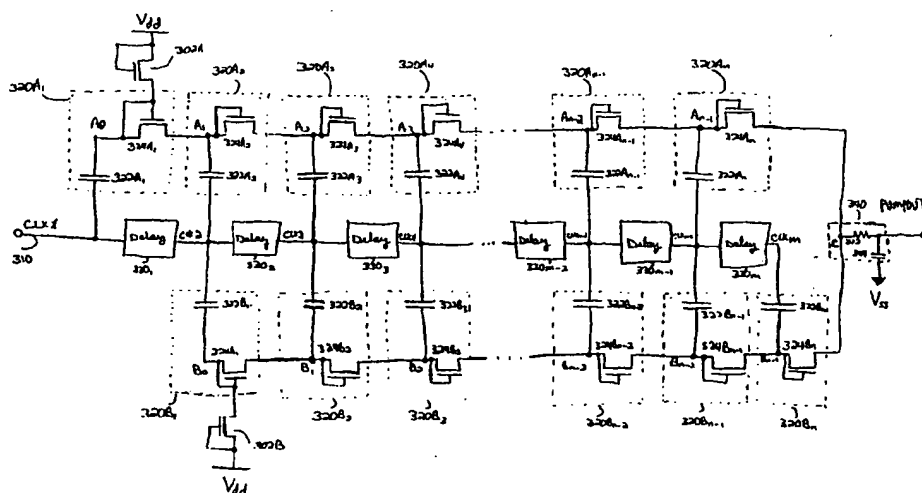
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(54) Method and apparatus for reducing power supply current surges in a charge pump using a delayed clock line

(57) The present invention is a charge pump circuit to reduce and distribute power supply current surges. The charge pump circuit includes a first clock line to provide a first clock thereon, a plurality of delay circuits connected in series, each delay circuit generating a delayed and inverted clock from its input clock on a respective output clock line, and a plurality of charge pump stages

connected in series each to store charge thereon. The first clock line is coupled to the first charge pump stage and the plurality of output clock lines are coupled to a respective plurality of remaining charge pump stages. The operation of each charge pump stage is staggered to reduce and distribute the power supply current surges.



300  
Figure 3A



European Patent  
Office

# EUROPEAN SEARCH REPORT

Application Number  
EP 98 30 7090

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 5 191 232 A (PING WANG) 2 March 1993 * abstract * * figure 2 * * column 1, line 44 - line 68 * * column 2, line 49 - line 56 * * column 4, line 45 - line 52 * * column 4, line 60 - line 65 * ---	1-10	H02M3/07
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CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document	

**ANNEX TO THE EUROPEAN SEARCH REPORT  
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